WHAT IS CLAIMED IS

1. A semiconductor integrated circuit, comprising:

a block having a first border edge on which an external connection terminal is provided and a second border edge on which no external connection terminal is provided;

a wiring prohibited area which extends a first distance from the first border edge and in which no wiring line running parallel to the first border edge exists; and

a shielding line which is at a second distance from the second border edge and runs parallel to the second border edge.

2. The semiconductor integrated circuit as claimed in claim 1, wherein said block is completely enclosed by border edges that are either the first border edge or the second border edge.

3. The semiconductor integrated circuit as claimed in claim 1, wherein said wiring prohibited area is situated inside the first border edge, and said shielding line is situated inside the second border edge.

4. The semiconductor integrated circuit as claimed in claim 1, wherein said wiring prohibited area is situated outside the first border edge, and said shielding line is situated outside the second border edge.

5. The semiconductor integrated circuit as claimed in claim 1, wherein said wiring prohibited area is situated inside and outside the first border edge, and said shielding line is situated inside and outside the second border edge.

6. The semiconductor integrated circuit as claimed in claim 1, wherein said block is a physical block that is a layout area divided on a function-by-function basis in hierarchical layout designing.

7. The semiconductor integrated circuit as claimed in claim 1, wherein the first and second border edges, the wiring prohibited area, and the shielding line are provided in a first wiring layer, and said block has a third border edge on which an external connection terminal is provided and a fourth border edge on which no external connection terminal is provided, the third and fourth border edges being provided in a second wiring layer that

is different from the first wiring layer, said semiconductor integrated circuit further comprising:

a wiring prohibited area which extends a third distance from the third border edge and in which no wiring line running parallel to the third border edge exists; and

a shielding line which is at a fourth distance from the fourth border edge and runs parallel to the fourth border edge.

8. A method of designing a semiconductor integrated circuit, comprising the steps of:

a) checking each border edge of a block area so as to determine whether a border edge is a first border edge where an external connection terminal is provided or a second border edge where no external connection terminal is provided;

b) providing a wiring prohibited area which extends a first distance from the first border edge and in which no wiring line running parallel to the first border edge exists; and

c) providing a shielding line which is at a second distance from the second border edge and runs parallel to the second border edge.

9. The method as claimed in claim 8, further comprising a step of cutting out a physical block as said block area, said physical block being a layout area divided on a function-by-function basis at a top level in hierarchical layout designing.

10. The method as claimed in claim 8, wherein said steps a) through c) are repeated with respect to each wiring layer.

11. The semiconductor integrated circuit as claimed in claim 1, wherein the first distance is longer than a minimum wiring distance.

12. The semiconductor integrated circuit as claimed in claim 1, wherein the second distance is equal to a minimum wiring distance.

13. The semiconductor integrated circuit as claimed in claim 7, wherein the third distance is longer than a minimum wiring distance.

14. The semiconductor integrated circuit as claimed in claim 7, wherein the fourth distance is equal to a minimum wiring distance.

15. The method as claimed in claim 8, wherein the first distance is longer than a minimum wiring distance.

16. The method as claimed in claim 8, wherein the second distance is equal to a minimum wiring distance.